Design, Implementation and Verification of a Customizing IP Soft Core with FPU Support

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Reconfigurable Hardware

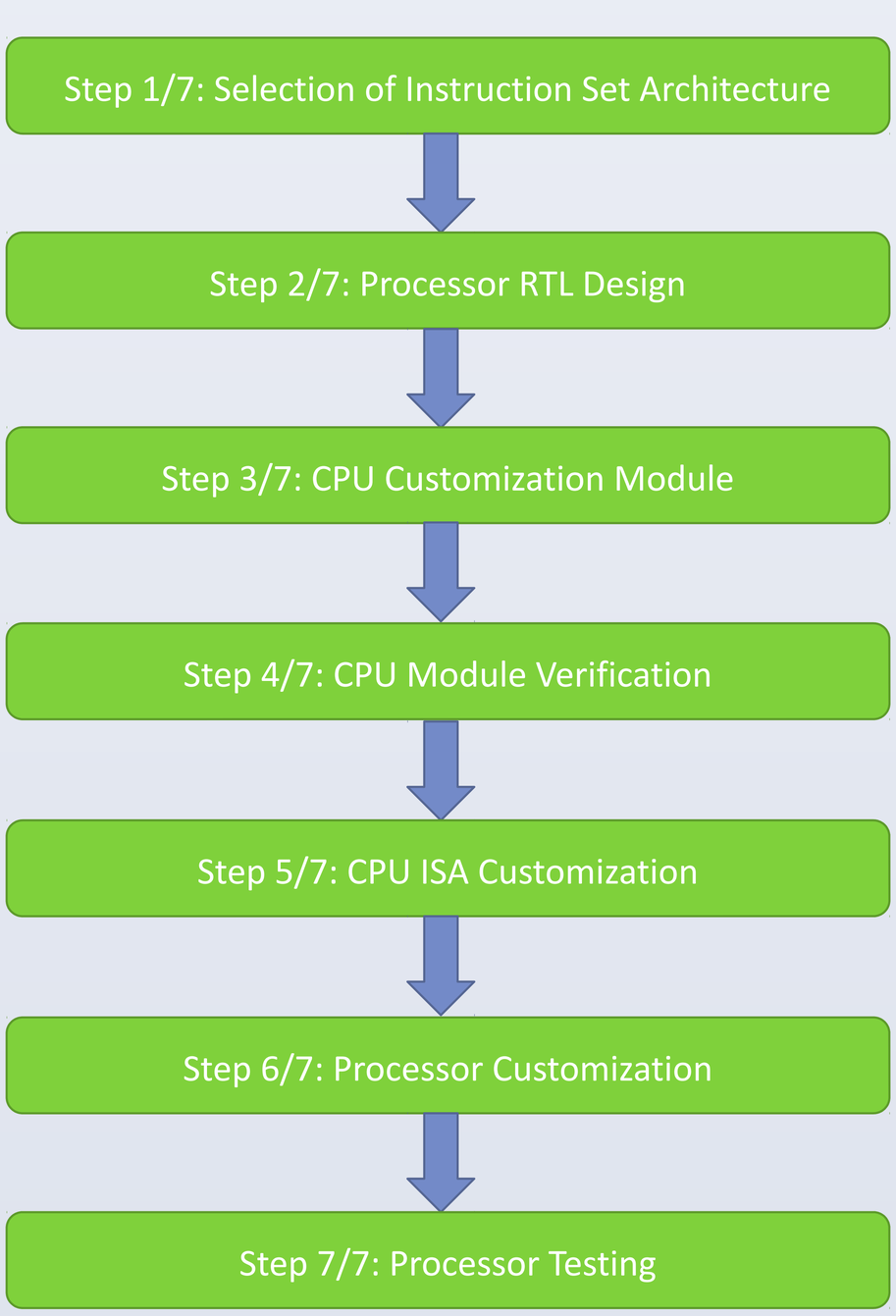
- Flexibility
- Low production cost
- Can be programmed with Hardware Description Languages.
- Customizable soft cores
- Easily adaptable
- Can be transferred and used in multiple platforms.

Key Features of our Work

In this research work, we present and analyze our web re-configurable IP-Core design flow, using as a test case the creation of a full soft core CPU and augmenting it with a double precision FPU. The key factor and motivation for this project was to present a simple and sufficient way of customizing large scale projects with IP-Cores and modules. We explain how to exploit this flexibility in an efficient way, with the creation of a web front-end, which enables every Internet user to customize this processor and download the VHDL description.

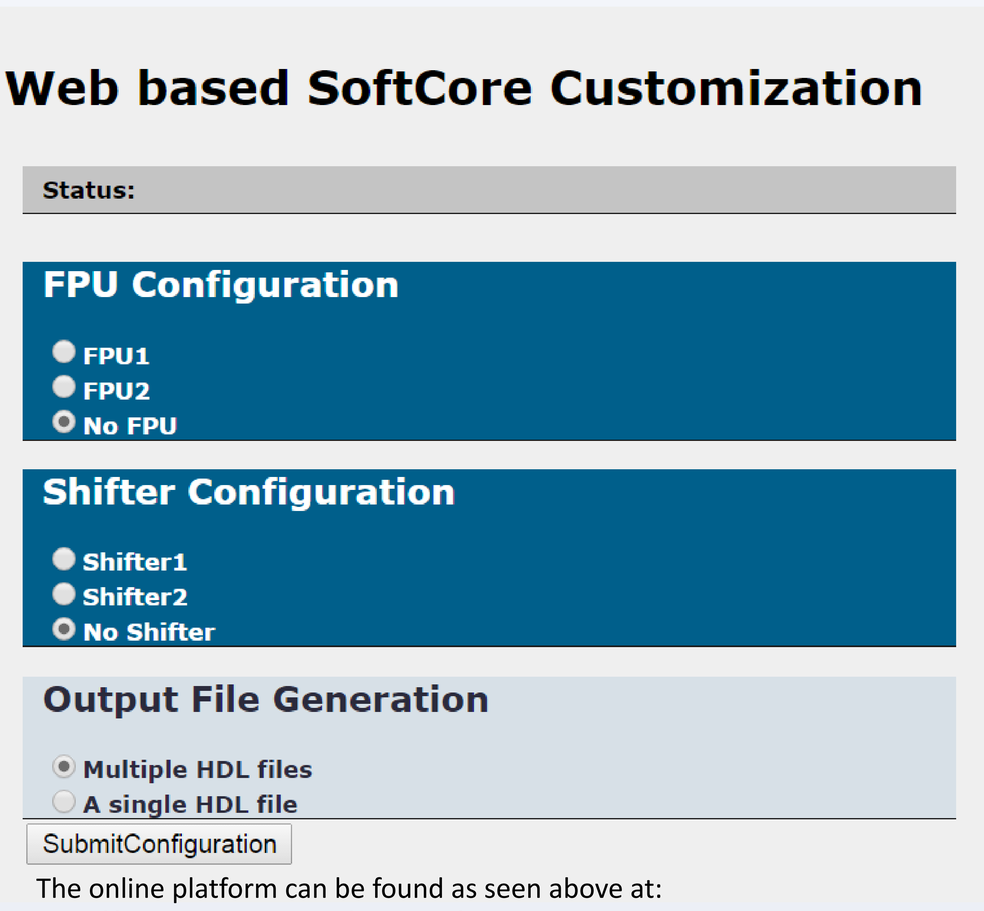
Design Flow

To customize the processor by embedding a new module in the most efficient way a design flow has to be followed. This design consists of seven steps, which provide a solid guideline for the designer and are presented below.



Web Configuration

In order to better support the flexibility and help the whole testing process, we have created a web based platform, where a designer can choose the modules to be included in the final design. The user selects the appropriate options and these requirements are processed to create the synthesizable soft core IP. The control logic of the processor is preprogrammed to support all the modules that are available, however this is the first step to the goal, which is to create a self-adapting control unit.



The online platform can be found as seen above at:
http://arch.icte.uowm.gr/cpucore/

Experimental Results

- We used the Virtex ML605 board.
- We performed the synthesis with Xilinx ISE 14.3.
- We performed the simulation with Modelsim PE Student edition 10.2c.
- We optimized all synthesis designs for timing performance.
- Maximum achieved frequency 58.289 MHz.
- Maximum IPS 52955260

Table 1 shows the metric results of our implemetation

Module	Max.Frequency	Op. Cycles	Area
Top Module	58.289 MHz	-	9% LUT Slices
Program Counter	294.638 MHz	1	<1% LUT Slices
Register File	382.117 MHz	1	4% LUT Slices
ALU	218.627 MHz	1/2/3/4	1% LUT Slices
FPU	81.155 MHz	1/2/3/5	<1% LUT Slices
MUL*	177.366 MHz	*	1% LUT Slices
MIX*	269.759 MHz	*	1% LUT Slices
Shifter*	133.832 MHz	*	1% LUT Slices

**These modules are combinational circuits and the maximum frequency has been calculated by the maximum propagation delay.*

Key Contributions

- We presented a detailed design description of a pipelined processor based on ISA PLX 1.1.
- Our enhancement of the processor by making it modular and easy to be customized.
- We created a web-based tool to provide a public platform for customizing and downloading the HDL files.

Future Work

- Creation of a “self adapting” control unit to utilize (unknown) user modules.
- Implement our methodology on a more popular soft processor such as LEON.